

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> ( Not for submission under 37 CFR 1.99)	Application Number		10550323
	Filing Date		2005-09-23
	First Named Inventor	Roger D. Chamberlain	
	Art Unit	2431	
	Examiner Name	Henning, Matthew T.	
	Attorney Docket Number	53047-57370	

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	4	5740244		1998-04-14	Indeck, et al.	
	5	5978801		1999-11-02	Yuasa	
	6	5995963		1999-11-30	Nanba et al.	
	7	6175874		2001-01-16	Imai et al.	
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	9	6389532		2002-05-14	Gupta et al.	
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20	7224185	B2	2007-05-29	Campbell et al.	
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	7	20040054924		2004-03-18	Chuah et al.	
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	13	20050187974	A1	2005-08-25	Gong	
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	18	20070118500		2007-05-24	Indeck et al.	
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	6	1999055052	WO		1999-10-28	Sun Microsystems, Inc.		<input type="checkbox"/>
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10	2002082271	WO		2002-10-17	Audible Magic Corporation		<input type="checkbox"/>
11	2003100662	WO		2003-12-04	Washington University		<input type="checkbox"/>
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13	2004042561	WO		2004-05-21	Lockheed Martin Corporation		<input type="checkbox"/>
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2	"Technology Overview", downloaded from the <a href="http://www.datasearchsystems.com/tech.htm">http://www.datasearchsystems.com/tech.htm</a> on April 19, 2004	<input type="checkbox"/>
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13	COMPTON ET AL., "Reconfigurable Computing: A Survey of Systems and Software", Technical Report, Northwestern University, Dept. of ECE, 1999, presented by Yi-Gang Tai	<input type="checkbox"/>
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24	International Preliminary Report on Patentability (Chapter II) for PCT/US2004/016021 dated August 21, 2007	<input type="checkbox"/>
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35	ROY, "A bounded search algorithm for segmented channel routing for FPGA's and associated channel architecture issues", IEEE, Nov. 11, 1993, pp. 1695-1705, Vol. 12	<input type="checkbox"/>
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